CHARACTERIZING CIRCUIT PERFORMANCE BY SEPARATING DEVICE AND INTERCONNECT IMPACT ON SIGNAL DELAY

ABSTRACT

An integrated circuit (IC) includes multiple embedded test circuits that all include a ring oscillator coupled to a test load. The test load either is a direct short in the ring oscillator or else is a interconnect load that is representative of one of the interconnect layers in the IC. A model equation is defined for each embedded test circuit, with each model equation specifying the output delay of its associated embedded test circuit as a function of Front End OF the Line (FEOL) and Back End Of the Line (BEOL) parameters. The model equations are then solved for the various FEOL and BEOL parameters as functions of the test circuit output delays. Finally, measured output delay values are substituted in to these parameter equations to generate actual values for the various FEOL and BEOL parameters, thereby allowing any areas of concern to be quickly and accurately identified.